

## **IV. Materials, Fabrication and Integration for Sensor Architectures**

### **(C2) Hybrid Molecular & Nanoscale CMOS-Based Architectures**

**Co-Chairs:** Victor Zhirnov, SRC, [victor.zhirnov@src.org](mailto:victor.zhirnov@src.org)  
Dev Palmer, U.S. ARO, [dev.palmer@us.army.mil](mailto:dev.palmer@us.army.mil)  
Rama Venkatasubramanian, RTI International, [rama@rti.org](mailto:rama@rti.org)

This session will focus on how novel nanoscale materials and devices, circuit concepts and sensor functionality can be integrated to develop new capabilities with possible applications to DoD Integrated and Networked Sensor Platforms. New concepts for devices, fabrication techniques, and system architectures are emerging. In particular, a wide range of new ideas have been proposed for post-CMOS technologies, such as molecular electronics, carbon nanotube devices, spin devices etc. Most likely, these options will yield their full potential only in combination with new and appropriate nanoarchitectures that integrate alternative electronic devices onto a silicon platform. Advantages may include: new approaches to reducing power levels; support for redundancies in sensing/computation/communication; fault tolerance; new functionality derived from CMOS and molecular components that form hybrid circuits; and ease of platform integration, all of which contribute to achieving the very aggressive weight, volume and cost targets of DoD (e.g., especially those needed in future unmanned military systems and sensor networks). Therefore, this session will seek to explore the potential payoffs that can be leveraged from integrating new emerging nanoelectronic devices into CMOS and CMOS-compatible platforms.